SEMESTER EXAMINATION, DECEMBER, 2025

Course Name: - B.TECH **Semester:-** THIRD

Paper Name: - Digital Electronics **Paper Code:-** NES 301

Time - 3 Hrs + 20 minutes per hour extra time for V.I. & examinees with writer. **Max Marks-70**

समय– 3 घण्टे 20 मिनट प्रति घंटे अतिरिक्त–दृष्टिबाधित एवं सह लेखक परीक्षार्थियों के लिए। अधिकतम अंक–70

Instructions:

- The question paper consists of three sections namely A, B, C. All sections are compulsory.
- Section A- Each question carries **3 mark. All questions are compulsory**.
- Section B- Answer any **5 out of 7** given questions. Each question carries **7 marks**.
- Section C- Answer any **2 out of 3** given questions. Each question carries **10 marks**.

Section – A (खण्ड–अ)

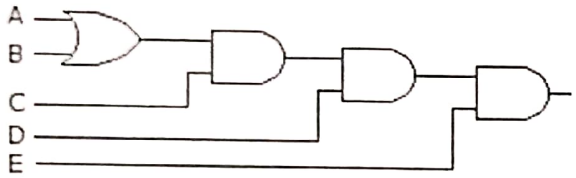
Multiple Choice Questions (बहुविकल्पीय प्रश्न)

1. Answer all the following questions. **5x3 =15**
निम्नलिखित सभी प्रश्न अनिवार्य हैं।

i) Convert binary (111111110010) to hexadecimal.

a) $(EE2)_{16}$
b) $(FF2)_{16}$
c) $(2FE)_{16}$
d) $(FD2)_{16}$

ii) Derive the Boolean expression for the logic circuit shown below:



a) $C(A + B)DE$

b) $\left[C(A + B)D + \overline{E}\right]$

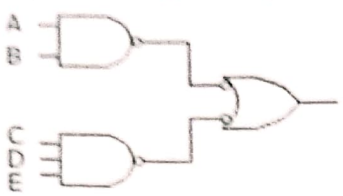
c) $\left[\left[C(A + B)D\right]\overline{E}\right]$

d) $ABCDE$

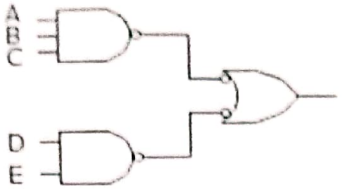
iii) Determine the values of A, B, C, and D that make the product term $\overline{A}B\overline{C}D$ equal to 1.

a) A = 0, B = 0, C = 0, D = 1
b) A = 0, B = 1, C = 0, D = 1
c) A = 1, B = 1, C = 1, D = 1
d) A = 0, B = 0, C = 1, D = 0

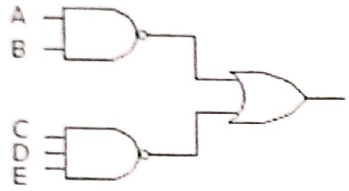
iv) Implementing the expression AB + CDE using NAND logic, we get:



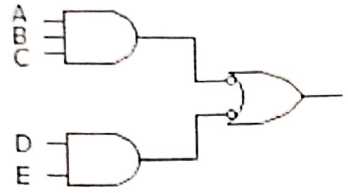
(A)



(B)

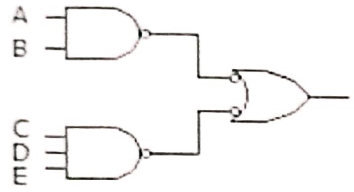


(C)

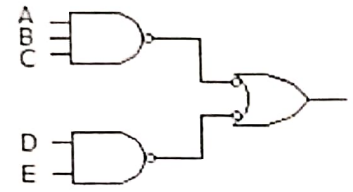


(D)

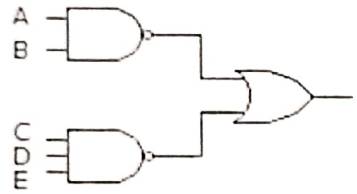
v) Implementing the expression $\bar{A} + \bar{B} + CD$ using NAND logic, we get:



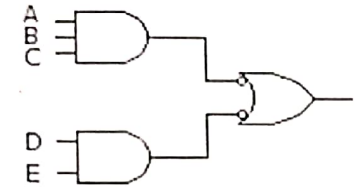
(A)



(B)



(C)



(D)

Section – B ;खण्ड–ब)

Short Answer Questions (लघुउत्तरीय प्रश्न)

2. Answer any five of the following questions. **5x7=35**
निम्नलिखित में से किन्हीं पाँच प्रश्नों के उत्तर दें।

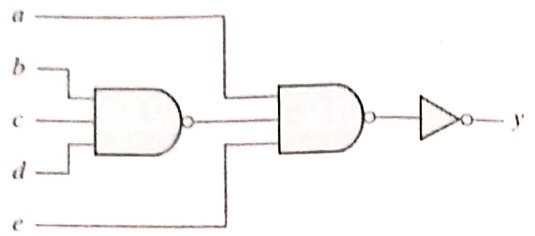
i. Given the two binary numbers X = 1010100 and Y = 1000011, perform the subtraction
(a) X - Y and
(b) Y - X by
Using **1's compliment**

ii. Using the K-map method, simplify the following functions:

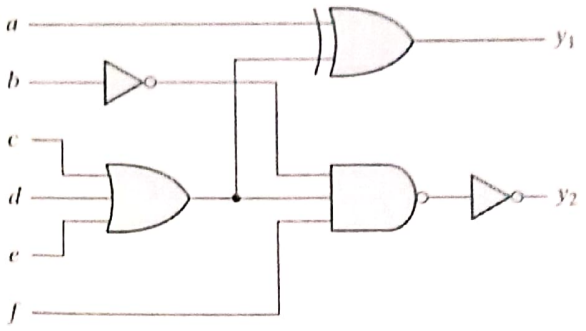
Minimum SOP of $\mathbf{f(w, x, y, z) = \Sigma(1,3,4,5,6,7,9,12,13)}$

Minimum POS of $\mathbf{f(w, x, y, z) = \Sigma(1,5,6,7,11,12,13,15)}$

iii. Write Boolean expressions and construct the truth tables describing the outputs of the circuits described by the logic diagrams



(a)



(b)

iv. Consider the multilevel Boolean function $\mathbf{F = (AB' + A'B)(C + D')}$ express using
(i) AND–OR gates (ii) NAND gates

v. How Combinational circuits differ from sequential circuits? Explain with suitable example.

vi. Draw the logic diagram corresponding to the following Boolean expression without simplifying it:

$$\mathbf{F = D + BC + (D + C')(A' + C)}$$

vii. Design **clocked D-Flip – Flop** using **NAND S-R Flip-Flop**, with complete expressions and trout table.

Section – C (खण्ड–स)
Descriptive Questions (विवरणात्मक प्रश्न)

3. Answer any two of the following question. **2x10=20**
निम्नलिखित में से किन्हीं दो प्रश्नों के उत्तर दें।

i) Obtain the minimal sum of products expression for the following function and implement the same using only NOR gates: **f(A,B,C,D)=Σ(0,2,3,5,6,7,8,9) with (10,11,12,13,14,15)** as don't cares.

ii) Design BCD to Seven-Segment Decoder.

iii) Implement full adder in sum-of-products form and differentiate it with full adder with two half adders for at least four bit input.

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